Thesis for the degree of Doctor of Philosophy

Design of ultra-low-voltage and ultra-low-power analog integrated circuits

by

Zhigang Qin

Graduate School of Electronics Engineering

Saitama Institute of Technology

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Abstract

In recent years, as a result of the electronic devices in the medical field, the automobile electron system, the military astronautics domain, the smartphones and tablet's widespread application, the demand for efficient low-power circuits is increasing just as rapidly due to the required battery operations of these handheld devices. Such applications usually require analog and mixed-mode circuits. One of the most important building blocks in analog and mixed-mode circuits is the operational amplifier (op-amp). In analog circuits, the current reference circuit influences on various features of the whole circuit.

The thesis has done the widespread investigation and study to the domestic and foreign technologies of analog low voltage circuits, and analyzed the principles of work, merits and shortcomings of these technologies. It designs a high performance operational amplifier. This article mainly aim at reducing the power consumption to launch the research and design operational amplifier. We develop and fabricate a 0.5-V rail-to-rail op-amp with ultralow-power operation in a 0.18-μm standard complementary metal-oxide-semiconductor (CMOS) process.

The op-amp has a two-stage structure that comprises a complementary input stage and a novel cross-coupled output stage. The structure of input stage adopted folded – cascode, and it has a large common-mode input range. The cross-coupled output stage increases the transconductances of the MOSFETs of the output stage without requiring additional chip area. Hence, it increases the gain of the op-amp and drivability for a capacitive load. Our experimental results showed that the DC gain was 77 dB at the common-mode input voltage of 0.25 V with a supply voltage of 0.5 V. DC gains of more than 40 dB were obtained for common-mode input voltages ranging 50−450 mV. Furthermore, the unity-

gain frequency was 4.0 kHz and phase margin was 56° with a capacitive load of 40 pF. The power consumption was 70 nW including all bias circuits.

In this thesis, a resistor-less reference circuit for ultra-low-voltage and ultra-low-current large-scale integrations is also proposed. It operates in nano ampere orders of current under the condition that the power supply is less than 1 V. At a supply voltage of 0.6 V, it provides a current of 2 nA, and the power consumption is 4.9 nW. In order to reduce the NMOS transistor's gate-source voltage and the threshold voltage, we connect the gate terminal with body terminal. And we use a deep-Nwell process in the standard process. The line regulation of proposed low-voltage current reference circuit is reduced to 18.3%/V with the supply voltage ranging from 0.6 to 1.8 V. For the layout design we used the Cadence layout software, and optimized the layout design to implement test chips. The layout area was $0.022\ \mathrm{mm}^2$.

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Design of ultra-low-voltage and ultra-low-power analog integrated circuits

Chapter 1

Introduction

1.1 Thesis Introduction

Microelectronic technique, electronic technology and computer technology with the close relations of mutually permeating, supporting and promoting each other, have gotten development at high speed. Analog and digital circuits with ultra-low power consumption can be widely used in many areas of applications. With the continuous development of deep-submicron technology, the voltage of power supply becomes lower and lower. It is very essential to study the design of low voltage and low power reference resource based on standard CMOS process [1].

At present, the low voltage low power CMOS analog integrated circuit and the current mode circuit with a great deal of merits are concerned very much by theory researchers and project engineers for VLSI technology.

Operational amplifier is widely used in all kinds of analog and mixed–mode circuit. As the industry moves towards lower power supply voltages, more and more people put their effort on the study of low-voltage precision op-amp. The lower supply also makes the dynamic range of signal reduced. This requires the op-amp a rail-to-rail input stage, In this thesis, designs of a ultra-low voltage,

nano-power rail-to-rail input stage CMOS operational amplifier and a ultra-low current reference circuit are described.

1.2 Thesis Outline

Chapter 2 of this thesis describes fundamentals of CMOS analog circuit design. It begins with a description of device in analog and digital CMOS processes. Then, Transistors in their weak-inversion saturation regions are introduced. In addition, the current sources and current mirrors are described.

Chapter 3 describes the background of this research work. Early work and applications are also discussed. Then, we proposed a rail-to-rail op-amp circuit, and described of simulation and experimental results.

In Chapter 4 the concept of ultra-low-voltage and ultra-low current reference circuit is introduced, and simulation results obtained from the new circuit are also shown.

Finally, Chapter 5 contains a summary of the work and plans for future work.

Chapter 2

Fundamentals of Analog Design and CMOS Integrated-Circuit Technology

In this chapter, devices in analog and digital CMOS processes are described. Then, transistors in their weak-inversion saturation regions are introduced.

2.1 Introduction

Integrated circuit design is separated into two major categories: analog and digital. An analog signal is a signal that is defined over a continuous range of time and a continuous range of amplitudes. Circuit design is the creative process of developing a circuit that solves a particular problem. Design can be better understood by comparing it to analysis [2].

2.2 MOS transistor structure

Simplified structure of a p-type MOS device shown in Fig. 2.1. The structure is symmetric with respect to source and drain. The device consists of two heavily-doped n - type regions forming the source and drain terminals, a heavily-doped piece of polysilicon operating as the gate, and a thin layer of silicon dioxide (SiO_2) insulating the gate from the substrate.

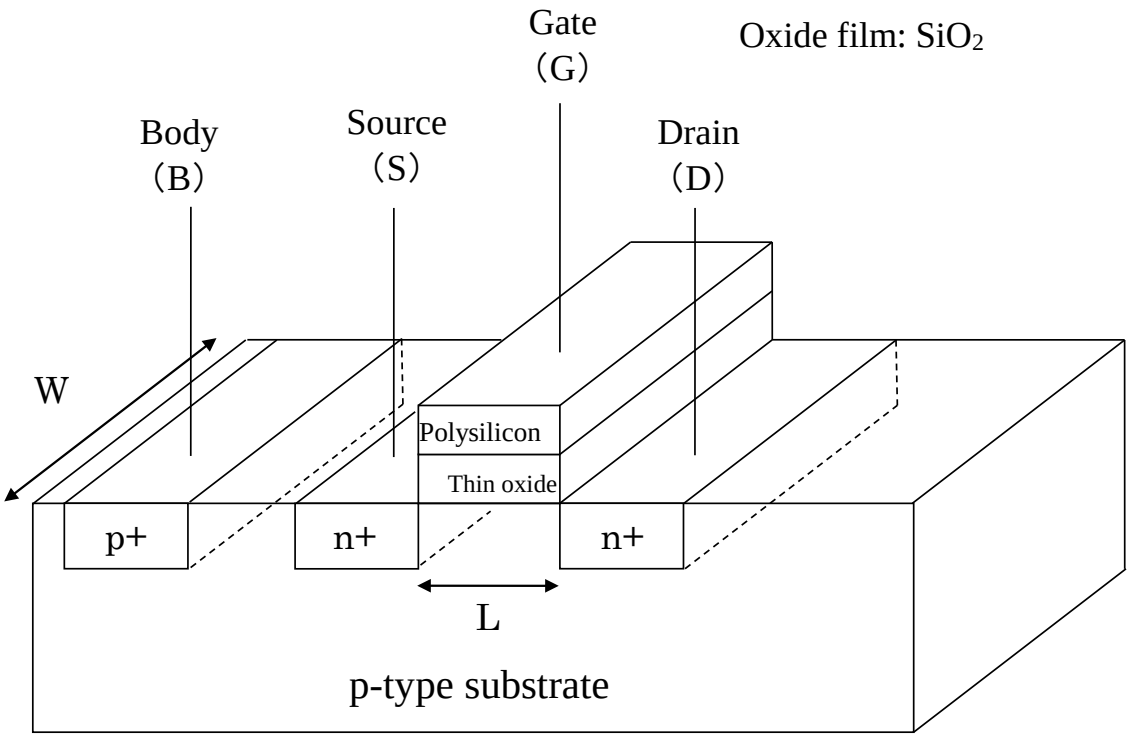


Fig. 2.1. Structure of a MOS device.

2.3 Weak Inversion in CMOS Transistors

The device operates in weak inversion when gate-source voltages less than the extrapolated threshold voltage V_T but high enough to create a depletion region at the surface of the silicon.

In the weak inversion region, the drain current is

$$I_D = I_0 \frac{W}{L} exp\{\frac{q(V_{GS}-V_T)}{nkT}\}\left\{1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right\}, \quad (2.1)$$

where I_o is a process-dependent parameter.

2.4 Current Sink and Current Mirrors

Current sink is realized by an NMOS transistor as shown in Fig. 2.2. And its current-voltage characteristic is shown in Fig. 2.3. The voltage across the current sink must be larger than Vmin in order for the current sink to perform properly.

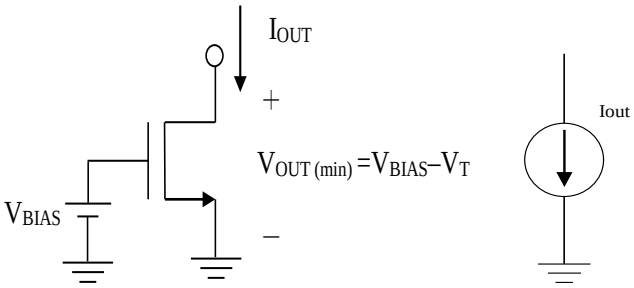


Fig. 2.2. Current sink [3].

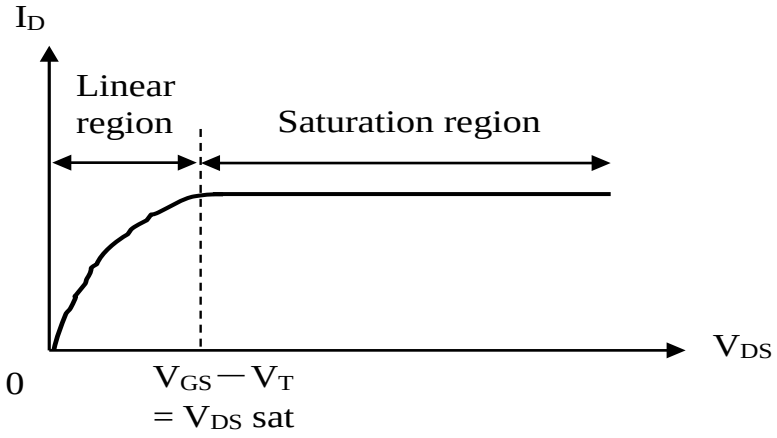


Fig. 2.3. Current-voltage characteristics ($I_D - V_{DS}$) [2].

A simple CMOS current mirror shown in Fig. 2.4. In analog circuits, the design of current sources is based on “copying” currents from a reference, with the assumption that one precisely-defined current source is already available [1].

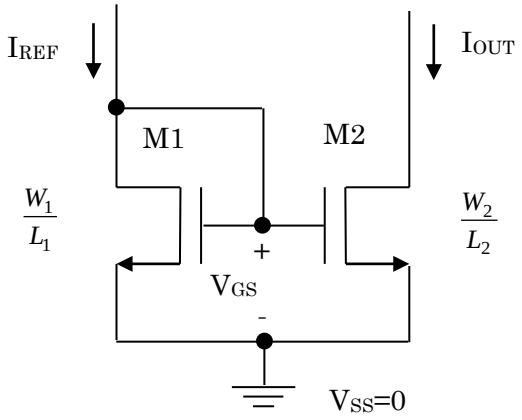


Fig. 2.4. A simple CMOS current mirror [1].

The drain-gate voltage of M1 is zero. The transistor M1 operates in the saturation or active region if the threshold is positive.

M1 and M2 operate in the saturation region. Their currents are given by

$$I_{REF} = \frac{1}{2}\mu_n C_{OX}\frac{W_1}{L_1}(V_{GS} - V_{TN})^2(1+\lambda V_{DS1}), \tag{2.2}$$

$$I_{OUT} = \frac{1}{2}\mu_n C_{OX}\frac{W_2}{L_2}(V_{GS} - V_{TN})^2(1+\lambda V_{DS2}). \tag{2.3}$$

In the most general case, the ratio of I_{OUT} to I_{REF} is

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W_2}{L_2}(1+\lambda V_{DS2})}{\frac{W_1}{L_1}(1+\lambda V_{DS1})}. \tag{2.4}$$

Neglecting channel-length modulation, we can write

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = \frac{W_2 L_1}{W_1 L_2} \tag{2.5}$$

obtaining (if $L_1=L_2$)

$$\frac{I_{OUT}}{I_{REF}} = \frac{W_2}{W_1}. \tag{2.6}$$

Consequently，the ratio of I_{OUT}/I_{REF} is given by the ratio of device dimensions. It allows precise copying of the current with no dependence on process and temperature. Circuit designers also can control I_{OUT} /I_{REF} by the aspect ratios.

2.5 Cascode stage

The cascade of a common-source (CS) stage and a common-stage (CG) is called a “cascode” topology (The term cascode is believed to be acronym for “cascade triodes,” possibly invented in vacuum tube days.) [1]. Fig. 2.5 shows a cascode stage. It provides a high output impedance and reduces the effect of the Miller capacitance.

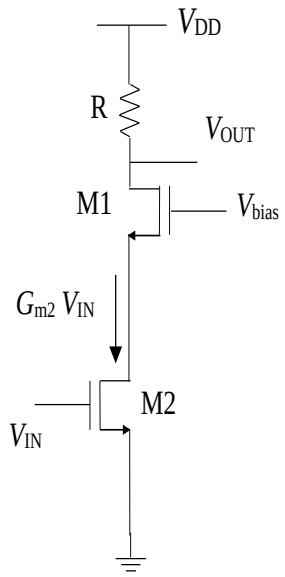


Fig. 2.5. Cascode stage.

2.6 Folded-cascode op-amp

The architecture show in Fig. 2.6 is commonly called the folded-cascode op-amp. This architecture was developed in part to improve the input common-mode range and the power-supply rejection of the two-stage op-amp. One of the advantages of the folded-cascode op amp is that it has a push-pull output [3]. In order to achieve a high voltage gain, the load of a folded-cascode can be implemented as a cascode itself [1].

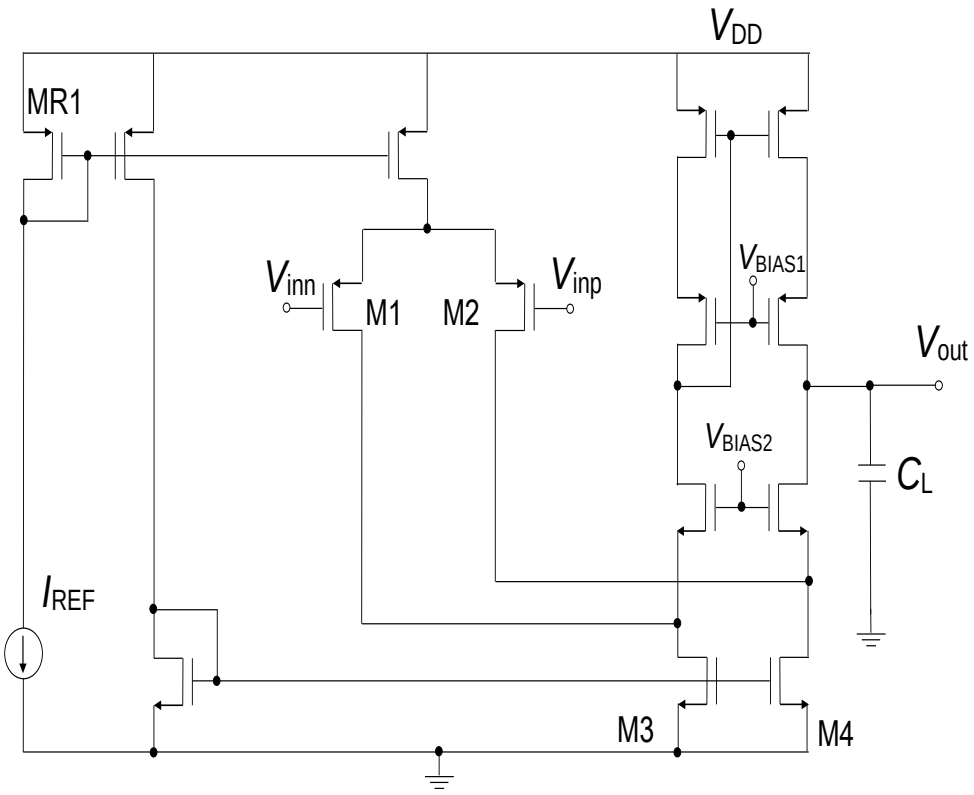


Fig. 2.6. Folded-cascode op-amp.

Chapter 3

Rail-to-Rail Operational Amplifier Using a Cross-Coupled Output Stage

3.1 Early Work and Applications

For more than a decade, low-voltage op-amps which operate with a supply voltage of 1V or below have been investigated [5-9]. Blalock proposed a body-driven input stage for a 1-V rail-to-rail op-amp [5], and Chatterjee realized a 0.5-V op-amp by using the body-driven technique [6]. However, the input impedance of these op-amps drop significantly when the pn junction of an input PMOS transistor, which consists of the source (p-type) and the body (n-type), is forward-biased. The circuit of [6] may get into the latch-up state when the supply voltage exceeds 0.7 V.

Stockstad proposed a buffered body-driven technique and realized a 0.9-V rail-to-rail op-amp [7], which operates up to 5.5 V. The input impedance is as high as that of a typical gate-driven CMOS op-amp. However, this circuit uses depletion-type NMOS transistors, which are usually not available in standard CMOS processes.

Lee used native NMOS transistors for the input pair of the first stage and realized a sub-0.5V rail-to-rail op-amp [8]. Native transistors can be realized without using extra masks, but minor process modifications are required.

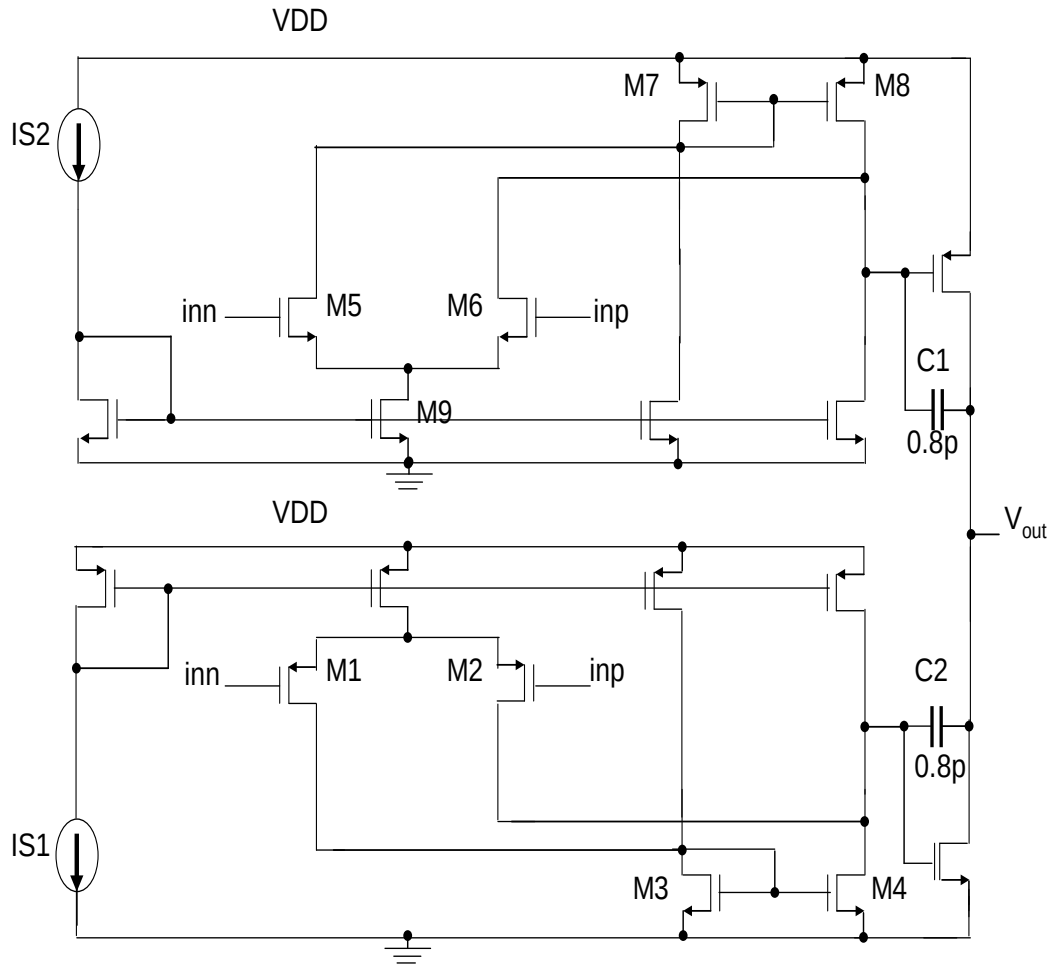


Fig. 3.1. Rail-to-Rail op-amp with a standard CMOS technology [9].

Takahashi proposed a 0.5-V rail-to-rail op-amp with a standard CMOS technology [9]. The first stage (i.e. the input stage) of this op-amp, shown in Fig. 3.1, are built using complementary (PMOS and NMOS) input pairs in parallel. The second stage consists of a common-source amplifier. The drawback of this circuit is that the input common-mode range is limited because of M3 and M7 in diode configurations, that is, their gate and drain are connected. Hence, it is hard to have a low drain-to-source voltage such as 100 mV unless the gate-to-source voltage is designed to be 100 mV.

3.2 Proposed circuit

In this brief, we describe a 0.5-V rail-to-rail CMOS op-amp. It has a large common-mode input range, which comprises a cross-coupled output stage to increase both the gain of the op-amp and drivability for a capacitive load. It can be realized in a standard CMOS process. The performance of the op-amp has been verified by HSPICE simulations. We have fabricated the op-amp using a standard CMOS process, and described the experimental results.

3.2.1 Input stage

Fig. 3.2 shows the proposed rail-to-rail op-amp. Unlike the circuit of [9], the gates of M3 and M7 are not connected to their drains. Therefore, V_{DS3} and V_{SD7} can be as small as 100 mV while keeping these MOS transistors in their weak-inversion saturation regions.

In the circuit of Fig. 3.1, the minimum common-mode input voltage, Vcmin (min), is

$$\text{Vcmin (min)} = V_{GS3} + V_{SD1} - V_{SG1} > 0 \text{ V}. \quad (3.1)$$

Assuming $V_{GS3} = V_{SG1}$, Vcmin (min) is higher than 0 V. It means that the common-mode input range does not cover the ground (0 V) in this structure. In the circuit of Fig. 3.2, on the other hand, the minimum common-mode input voltage is

$$\text{Vcmin (min)} = V_{DS3} + V_{SD1} - V_{SG1} < 0 \text{ V}. \quad (3.2)$$

Assuming $V_{DS3} = V_{SD1}$, Vcmin (min) can be lower than 0 V. Therefore, the common-mode input range covers the ground (0 V) in the proposed circuit.

The maximum common-mode input voltage, Vcmin (max), in the circuit of Fig. 3.1 is

$$\text{Vcmin (max)} = V_{DD} - V_{SG7} - V_{DS5} + V_{GS5} < V_{DD}. \quad (3.3)$$

In the circuit of Fig. 3.2, on the other hand, it is

$$\text{Vcmin (max)} = V_{DD} - V_{SD7} - V_{DS5} + V_{GS5} > V_{DD}. \quad (3.4)$$

Additionally the proposed circuit has a cascode structure in the first stage and a high voltage gain is expected.

Each MOSFET has been designed to have a gate-to-source voltage (V_{GS}) of 0.2 V. It is obvious that these MOSFETs operate in their subthreshold regions. Their drain-to-source voltages are kept more than 100 mV so that they stay in their saturation regions.

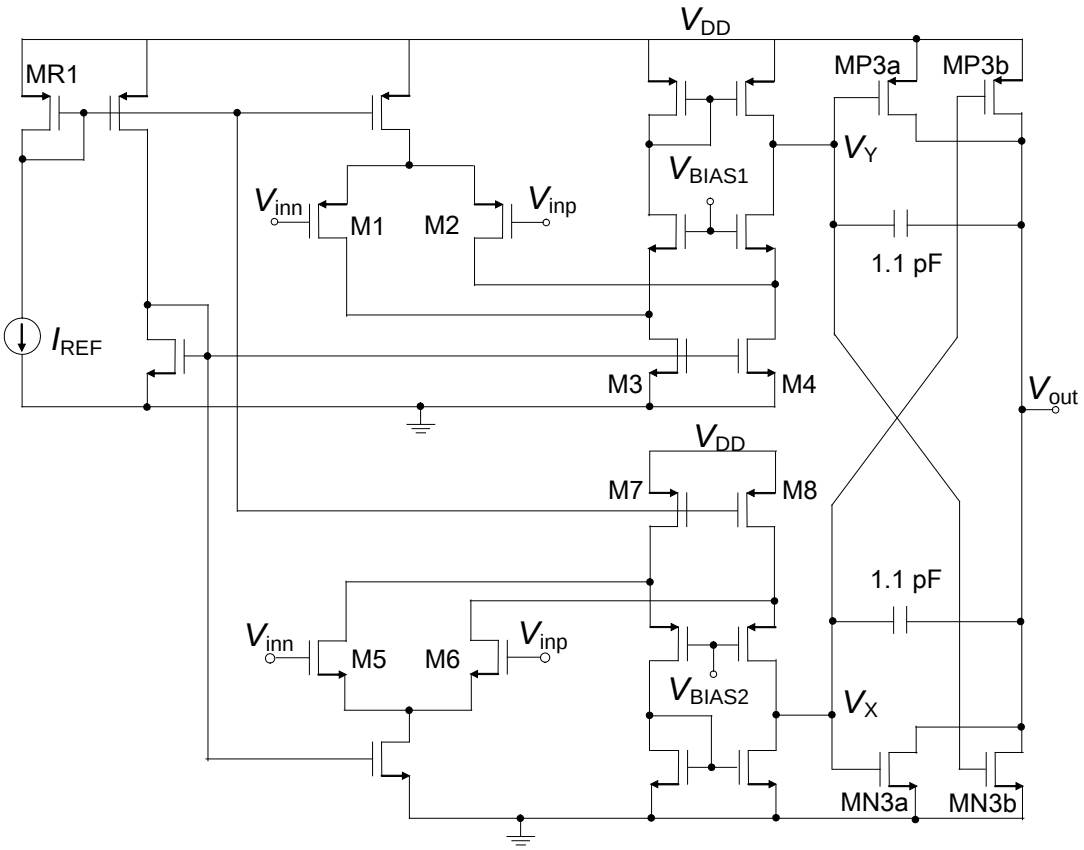


Fig. 3.2. Proposed rail-to-rail op-amp with a cross-coupled output stage.

3.2.2 Cross-coupled output stage

Fig. 3.3(a) shows a conventional common-source output stage. We assume here that both PMOS transistor MP3 and NMOS transistor MN3 comprise 10 unit transistors in parallel.

Fig. 3.3(b) shows our novel cross-coupled output stage [10]. Essentially, the PMOS transistor MP3 in Fig. 3.3(a) is divided in half and shown in Fig. 3.3(b) as MP3a and MP3b. Both MP3a and MP3b comprise five unit transistors in parallel. Similarly, NMOS transistor MN3 in Fig. 3.3(a) is also divided in half, as shown in Fig. 3.3(b) as MN3a and MN3b. Both MN3a and MN3b comprise five unit transistors in parallel. Therefore, the silicon area is unchanged in our new design.

In the following explanation, we assume that V_{DD} is 0.5 V. The gate terminal of MP3b is connected to the gate of MN3a, and the gate terminal of MN3b is connected to the gate of MP3a. For example, if V_{SG} of MP3a is set to 0.2 V, then V_{GS} of MN3b is 0.3 V. Furthermore, if V_{GS} of MN3a is set to 0.2 V, then V_{SG} of MP3b is 0.3 V. Because V_{GS} of MN3b and V_{SG} of MP3b are larger than those of the conventional common-source output stage shown in Fig. 3.3(a), the transconductances of these MOSFETs increase. Conversely, V_{GS} of MN3a and V_{SG} of MP3a are each 0.2 V that is similar to V_{GS} or V_{SG} of MOSFETs in the input stage.

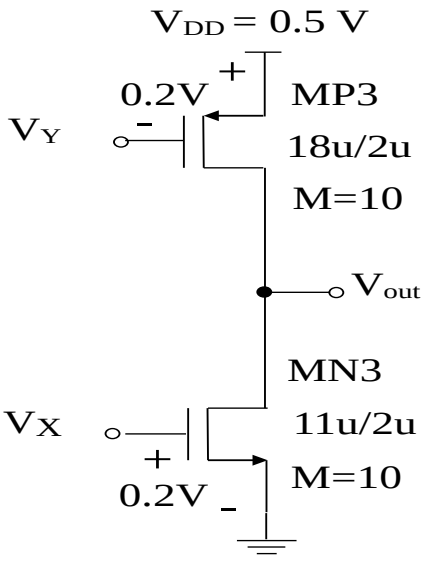


Fig. 3.3 (a). Conventional common-source output stage [18].

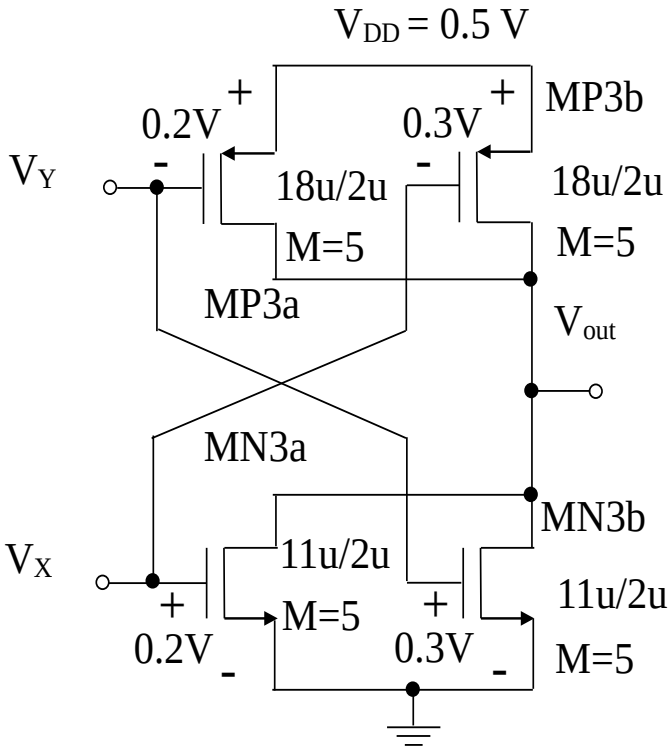


Fig. 3.3 (b). Proposed cross-coupled output stage.

is connected to V_Y, and the gate terminal of MP3 is connected to V_X. Although this structure increases the transconductance of the output stage, the quiescent current also increases significantly.

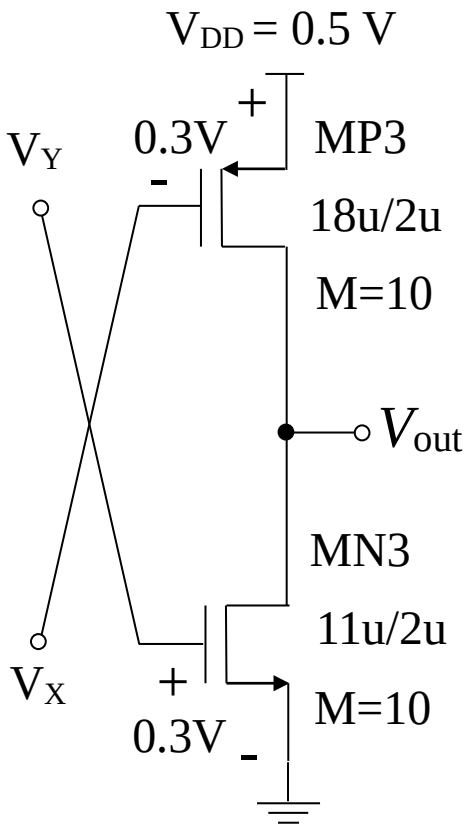


Fig. 3.3 (c). shows a fully cross-coupled output stage. The gate terminal of MN3.

As a conclusion, we expect that the cross-coupled output stage shown in Fig. 3.3(b) is the most useful among them. It increases the transconductance of MOSFETs of the output stage and enhances the gain of the op-amp and drivability for a capacitive load with moderate current consumption.

3.2.3 Reference-current generation circuit

Fig. 3.4 shows a current reference circuit. We have adopted the Oguey bias

circuit [10] to generate a reference current of 2 nA. Without using a resistor, a supply-voltage-independent current-reference circuit is realized.

M_{IREF} in Fig. 3.4 works as a current source (I_{REF}) in Fig. 3.2. MR2, MR3, MR4, MR5 and MR6 form the supply-independent bias circuit. Unlike a conventional bias circuit in which a resistor is used, an NMOS transistor MR6 is used for the resistor-free circuit [10].

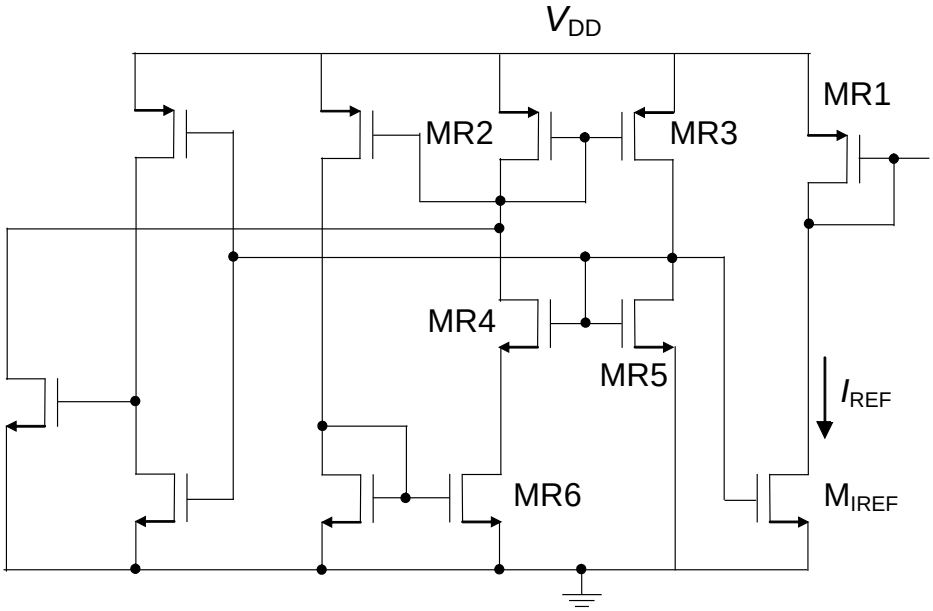


Fig. 3.4. Reference-current generation circuit [10].

3.3 Simulation Results

We have run HSPICE simulations for the proposed circuit shown in Fig. 3.2 using SPICE parameters for a standard 0.18-μm CMOS process with a supply voltage of 0.5 V. Bias circuits for V_{BIAS1} and V_{BIAS2} (not shown in Fig. .2) are also included in simulations. The threshold voltages for PMOS and NMOS are about –0.4 V and 0.45V, respectively.

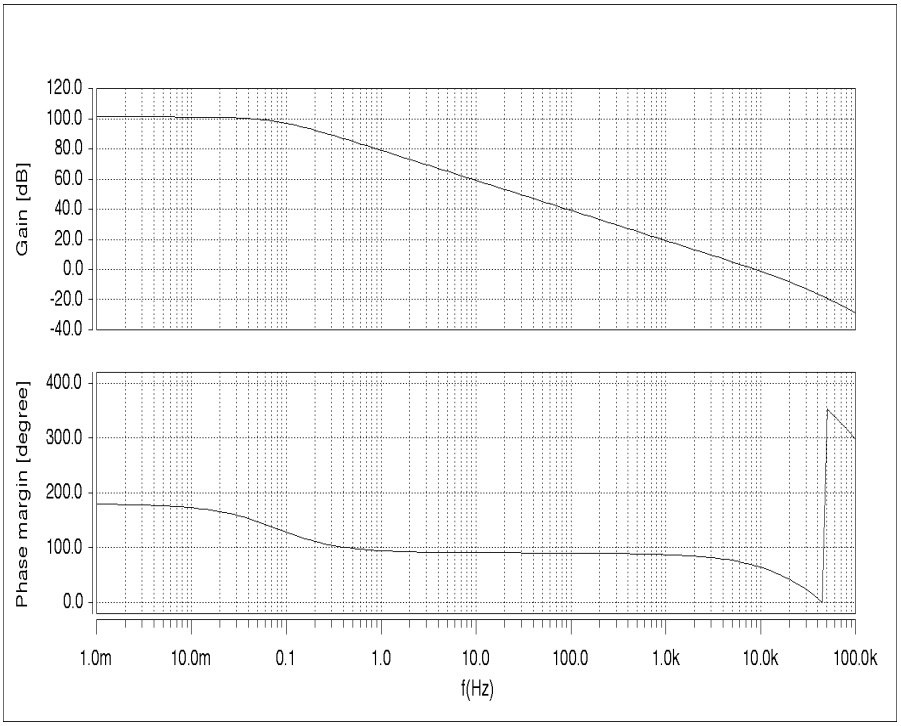


Fig. 3.5. Gain (above) and phase margin (below).

Fig. 3.5 shows the gain and phase margin at the common-mode input voltage of 0.25 V. The DC gain of the proposed op-amp is 101 dB, the unity-gain frequency is 8.2 kHz, and the phase margin is 50 degree with a load capacitance of 40 pF. The power consumption is 85 nW for the whole circuit including bias circuits.

To verify the common-mode input range, the difference between the input and output voltages in a voltage-follower configuration has been investigated. The result is shown in Fig. 3.6. The voltage difference between the input and output is within +/– 1 mV for the entire range from 0 V to 0.5V. (In this work, device mismatches and process corners have not been investigated yet.)

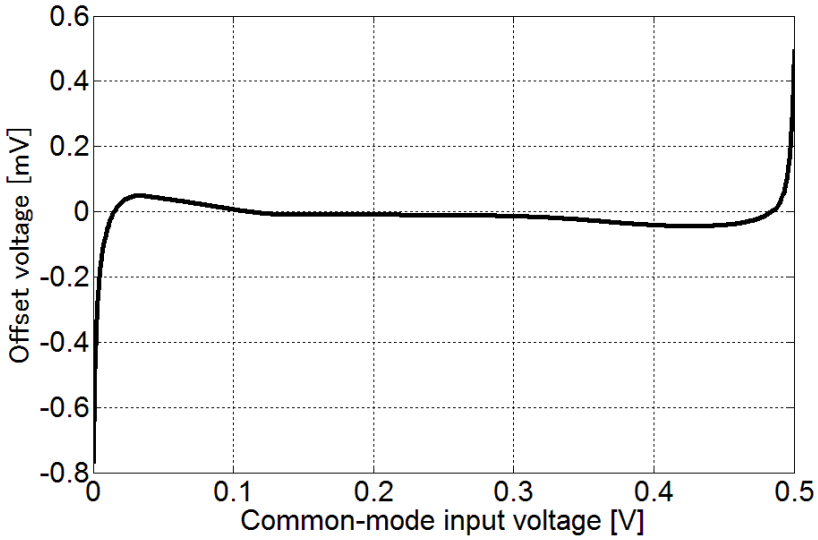
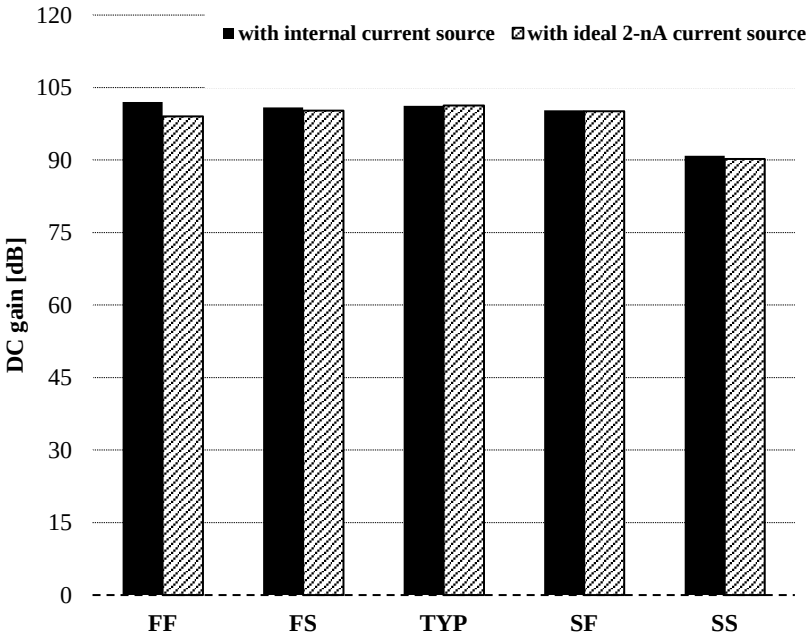
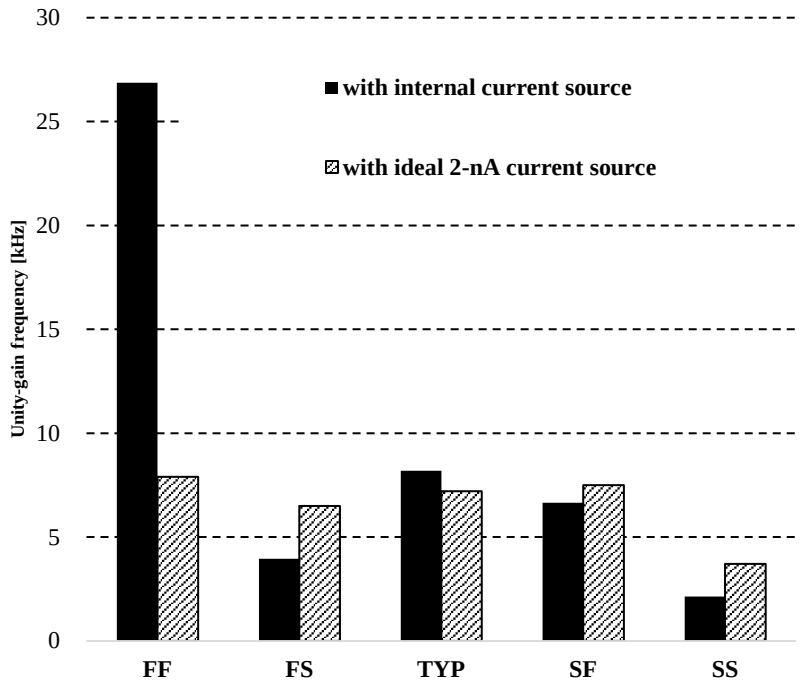


Fig. 3.6. Voltage difference between the input and output in a voltage-follower configuration.

To investigate the effect of process variations, we ran process corner simulations and the results are shown in Fig. 3.7. In Fig. 3.7, the notation F means fast and S means slow. For example, FS indicates a combination of fast NMOS and slow PMOS. The unity-gain frequency varied considerably by process conditions because our 2-nA reference current was affected a lot by process conditions. When the 2-nA current reference circuit was replaced by an ideal 2-nA current source, the variations in the op-amp performance were reduced. The robust design of the 2-nA reference current circuit is our future task.

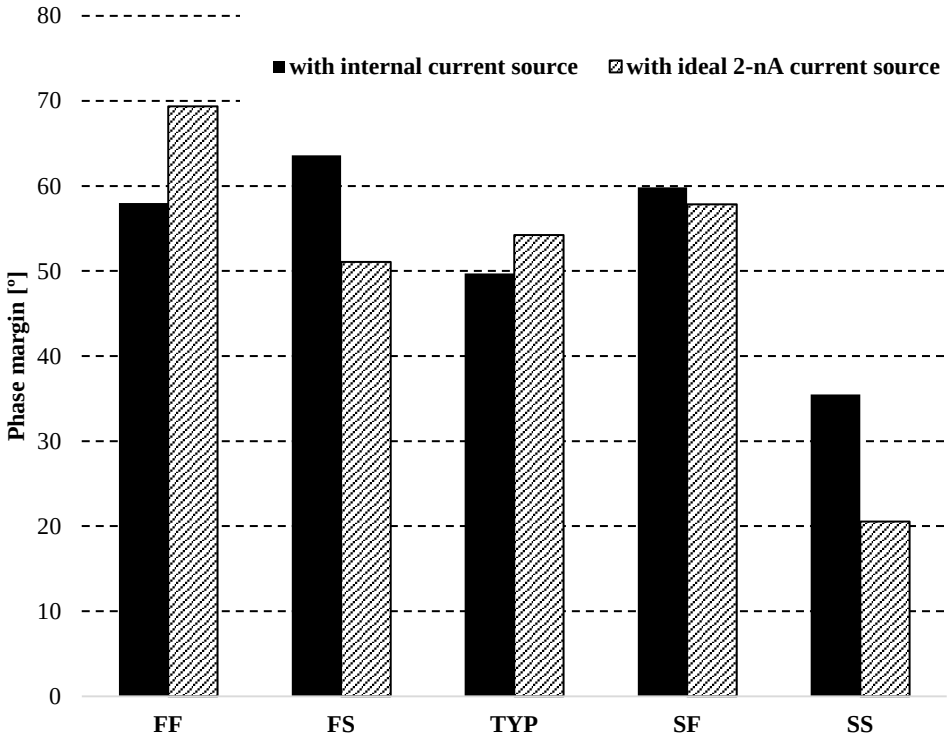


(a)



(b)

Fig. 3.7. Process corner simulations. (a) DC gain. (b) Unity-gain frequency.



(c)

Fig. 3.7. Process corner simulations. (c) Phase margin.

Fig. 3.8 shows the supply-voltage dependence of the total current consumption. For comparison, circuits using output stages of Figs. 2a and 2c are also shown. In the proposed circuit using the cross-coupled output stage of Fig. 2b, the total current increases to 774 nA at 0.6 V. In Fig. 2c, the total current was 1.34 μA at 0.6 V (It was 282 nA at 0.5 V). The supply-voltage dependence of total current consumption is a shortcoming of the cross-coupled output stage. However, the proposed circuit was developed for ultra-low voltage applications, such as 0.5 V, and is not suitable for a supply voltage larger than 0.5 V.

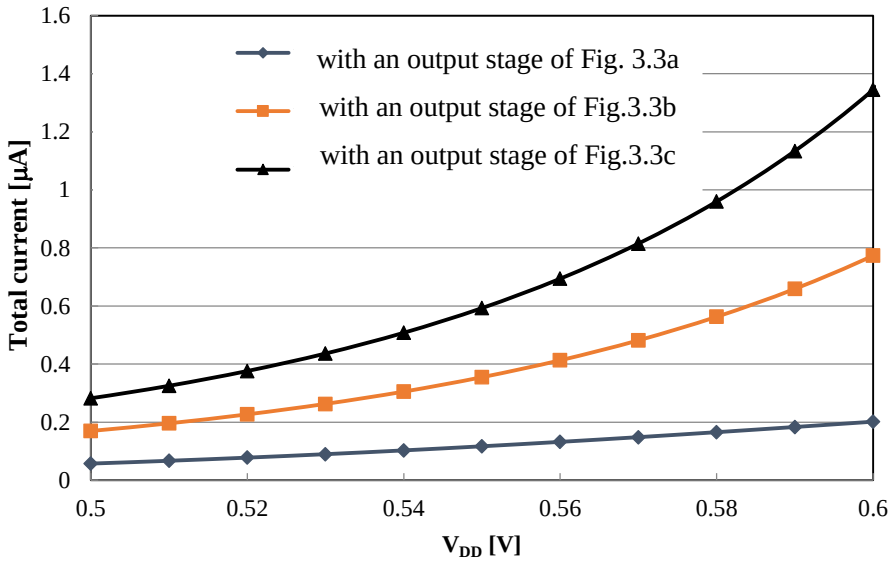


Fig. 3.8. Supply-voltage dependence of total current consumption.

Fig. 3.9 shows the DC gain with the common-mode input voltage. The proposed circuit has a DC gain of more than 80 dB for common-mode input voltages from 40 mV to 400 mV, and more than 60 dB from 32 mV to 467 mV. For comparison, the DC gain of an op-amp without the cross-coupled output stage (with a common-source output stage instead) is also shown in Fig. 3.9.

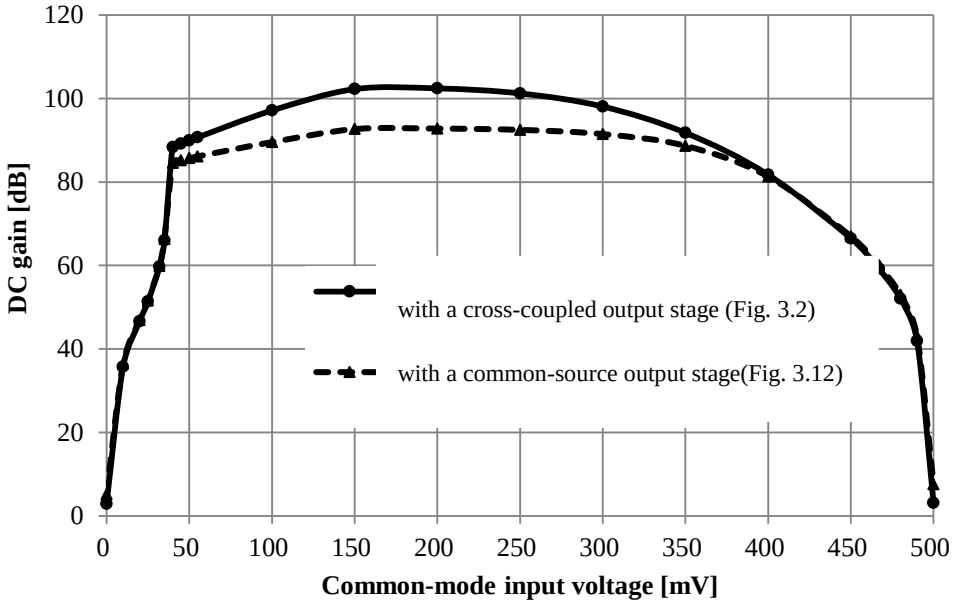


Fig. 3.9. DC gain and common-mode input voltage.

The transconductance of the input stage is shown in Fig. 3.10. Since the input stage consists of a PMOS pair and an NMOS pair, the total transconductance of the input stage depends on the common-mode input voltage. This is a subject for future.

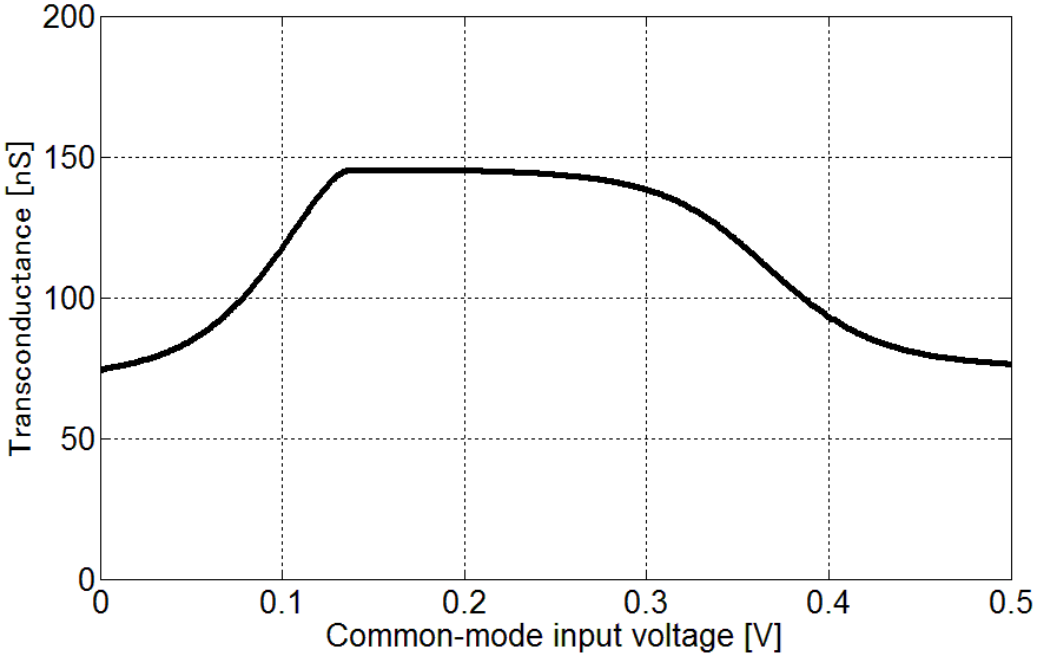


Fig. 3.10. Transconductance and the common-mode input voltage.

Common-mode rejection ratio (CMRR) is shown in Fig. 3.11. CMRR of 90 dB is obtained for low frequencies.

Figure of merit (*FoM*) is calculated using the equation described below,

$$FoM = \frac{UGF \cdot C_L}{I_{total}}, \tag{3.5}$$

where *UGF* is the unity-gain frequency, C_L is the load capacitance, and I_{total} is the current consumed in the whole circuit. *FoM* of the proposed circuit (including all bias circuits) is 1930 MHz · pF/mA with a load capacitance of 40 pF.

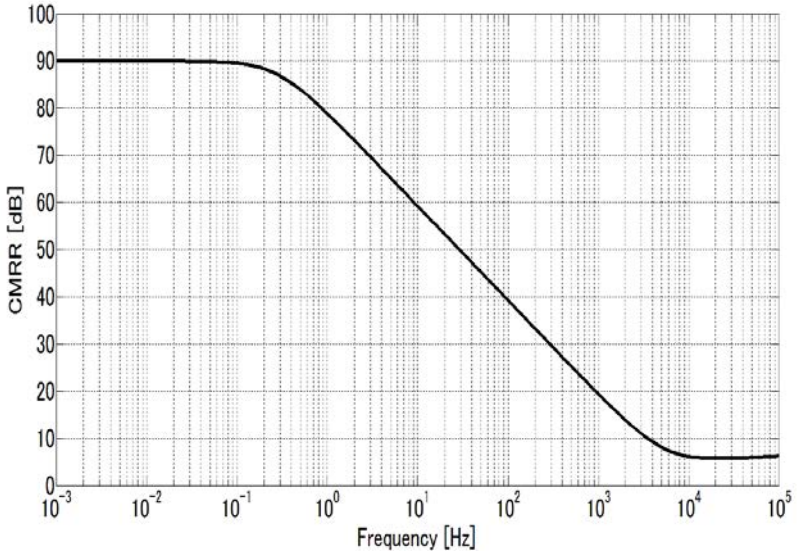


Fig. 3.11. Common-mode rejection ratio (CMRR).

Maximum sink current and source current at a supply voltage of 0.5 V are 52 μA and 23 μA, respectively.

For comparison, a rail-to-rail op-amp with a common-source output stage shown in Fig. 3.11 was simulated. With a load capacitance of 5 pF, the unity-gain frequency is 8.3 kHz and the phase margin is 49 degree (which is almost equal to the phase margin of the circuit shown in Fig. 3.2 with a load capacitance of 40 pF). With a load capacitance of 10 pF, the unity-gain frequency is 7.6 kHz and the phase margin is only 40 degree. The phase margin reduces because the second pole moves toward a lower frequency by increasing the load capacitance.

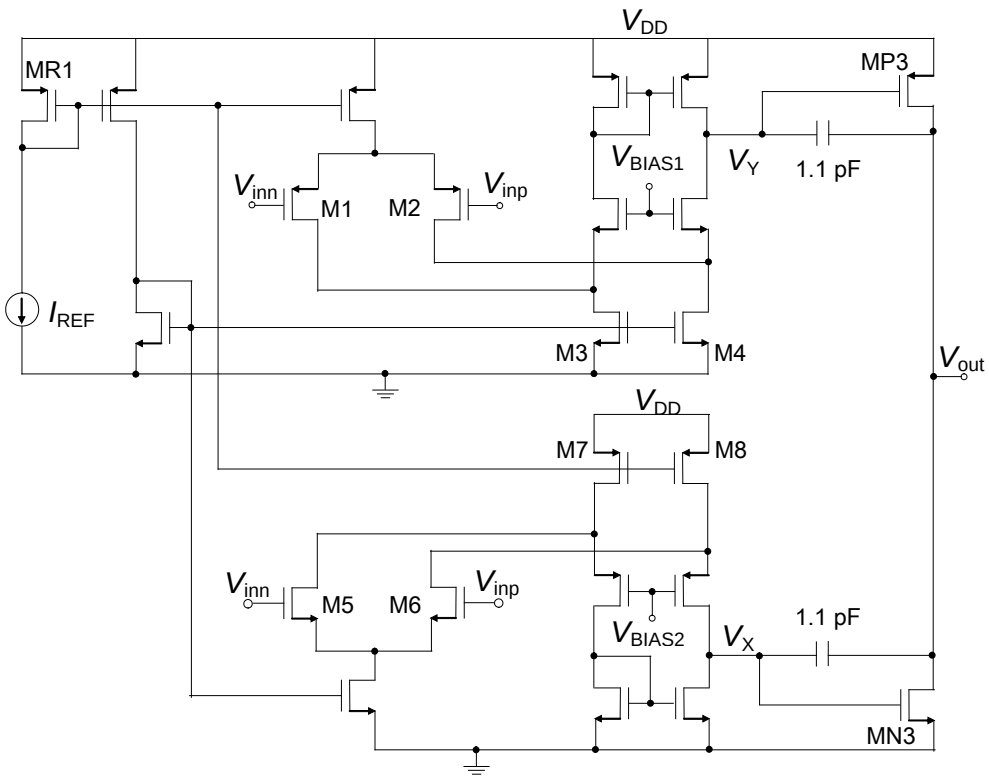


Fig. 3.12. Rail-to-rail op-amp with a common-source output stage.

On the other hand, in the proposed circuit (Fig. 3.2), the second pole locates at a higher frequency because the transconductance of the output stage is larger than that of Fig. 3.12. Therefore even with a capacitive load of 40 pF, a phase margin of 50 degree is obtained.

Fig. 3.13 shows simulation results of the current reference circuit used in the op-amp. The reference current was 2 nA at a supply voltage of 0.5 V. Because the reference current is not constant at a supply voltage of 0.5 V, the reference current circuit must be improved for future.

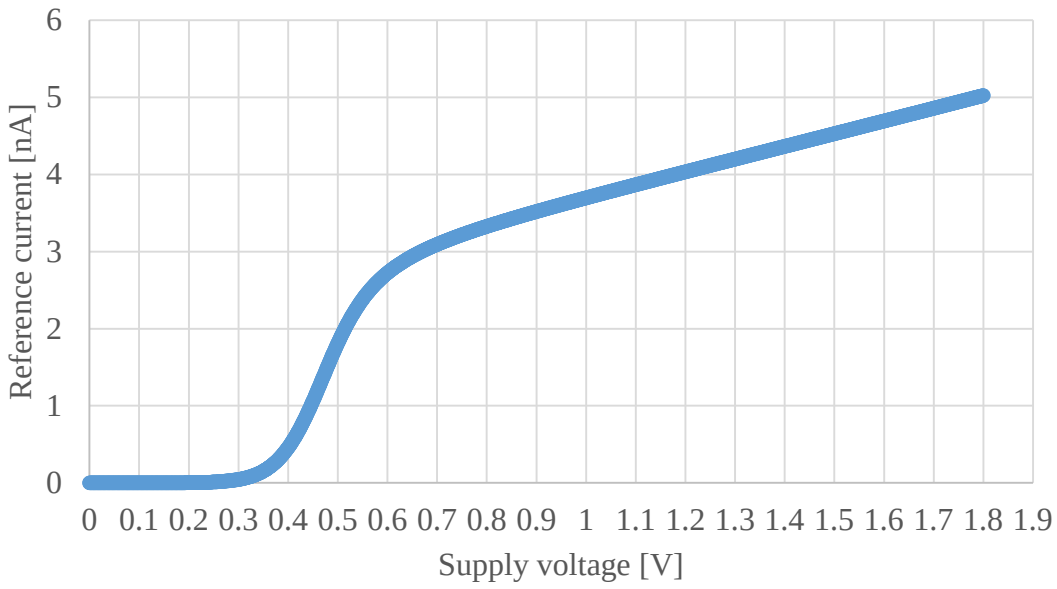


Fig. 3.13. Simulation result of the reference current circuit used in the op-amp.

Fig. 3.14 shows process variations of the reference current used in the op-amp. In Fig. 3.14, the first symbol represents the NMOS condition and the second symbol represents the PMOS condition. The symbol F means fast and S means slow. T represents typical. For example, FS indicates a combination of fast NMOS and slow PMOS. At a supply voltage of 0.5V, the reference current was affected a lot by process conditions. The robust design of the 2-nA reference current circuit which operates at 0.5 V is our future task.

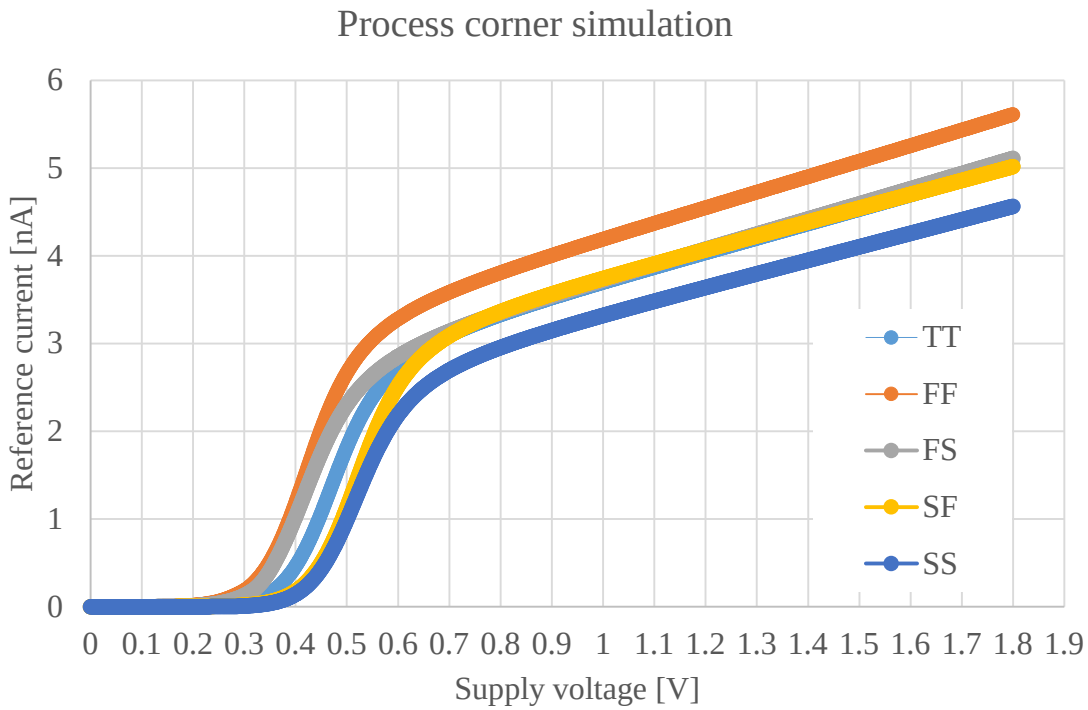


Fig. 3.14. Reference currents for process variations.

Table I summarizes simulation results of the proposed circuit with those of related circuits.

TABLE I SUMMARY OF SIMULATION/EXPERIMENTAL RESULTS [16]

	[1]*	[2]*	[3]*	[4]*	[5]**	This work with a cross-coupled output stage**	This work with a common-source output stage**
Supply voltage [V]	1.0	0.5	0.9	0.5	0.4	0.5	0.5
DC gain [dB]	49	62	79	62	63	101	92
Unity-gain frequency [kHz]	1,300	10,000	5.6	102	5.0	8.2/8.6	8.3
Load capacitance C_L [pF]	22	20	12	20	N/A	40/20	5
Phase margin [degree]	57	N/A	62	52	N/A	50/59	49
Supply current [μA]	300	150	0.5	3.0	0.02	0.17	0.057
Power [μW]	300	75	0.45	1.5	0.008	0.085	0.029
CMRR (at DC) [dB]	56**	N/A	59	N/A	N/A	90	90
Figure of Merit [MHz·pF/mA]	100	1330	130	680	N/A	1930/1010	730

*experimental results, **simulation results.

3.4 Integrated Circuit Layout and Experimental Results

We fabricated the proposed op-amp shown in Fig. 3.2 in a standard 0.18-μm CMOS process. The layout and die photograph of the op-amp are shown in Figs. 3.15 and 3.16, respectively. Excluding the 2-nA current reference circuit, the die area for the op-amp was 0.018 mm^2; similarly, the die area of the 2-nA current reference circuit was 0.018 mm^2.

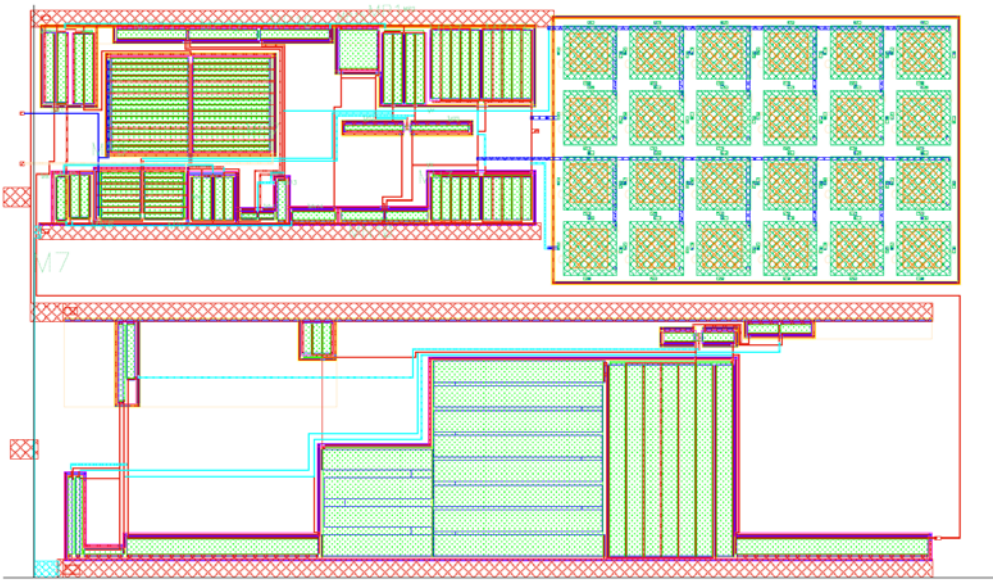


Fig. 3.15. Layout of the op-amp [18].

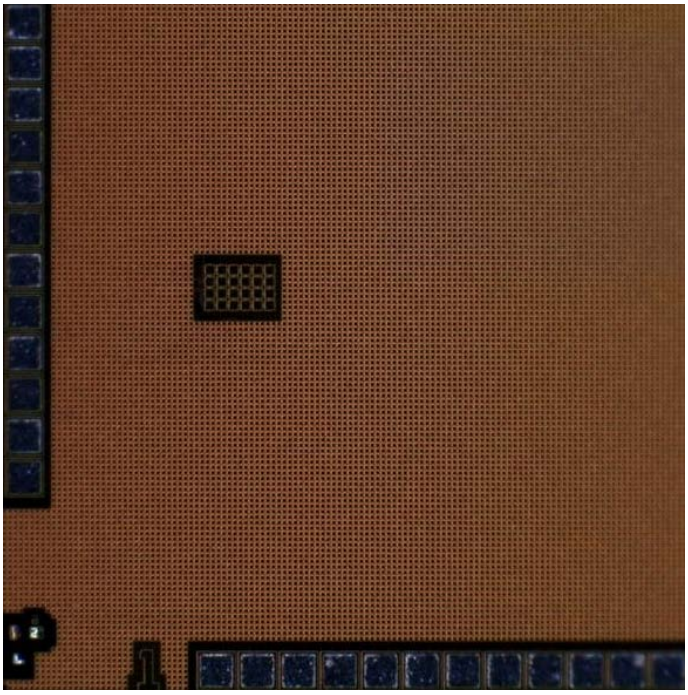


Fig. 3.16. Die photograph of the op-amp [18].

Fig. 3.17 shows the rail-to-rail input and output waveforms of the op-amp in a unity-gain buffer configuration with a 0.5-V supply voltage. A sinusoidal input signal with an amplitude of 0.5 V was supplied from the Tektronix AFG3022C function generator.

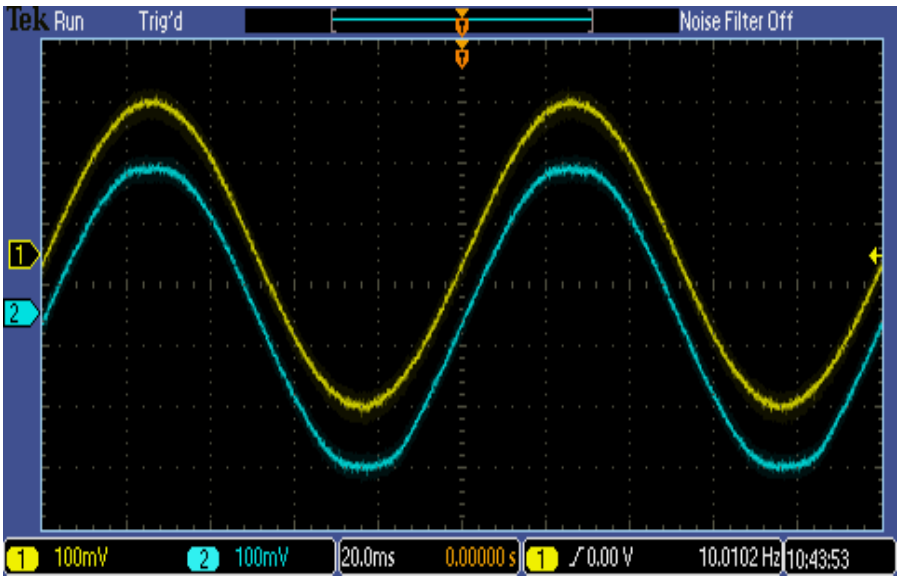
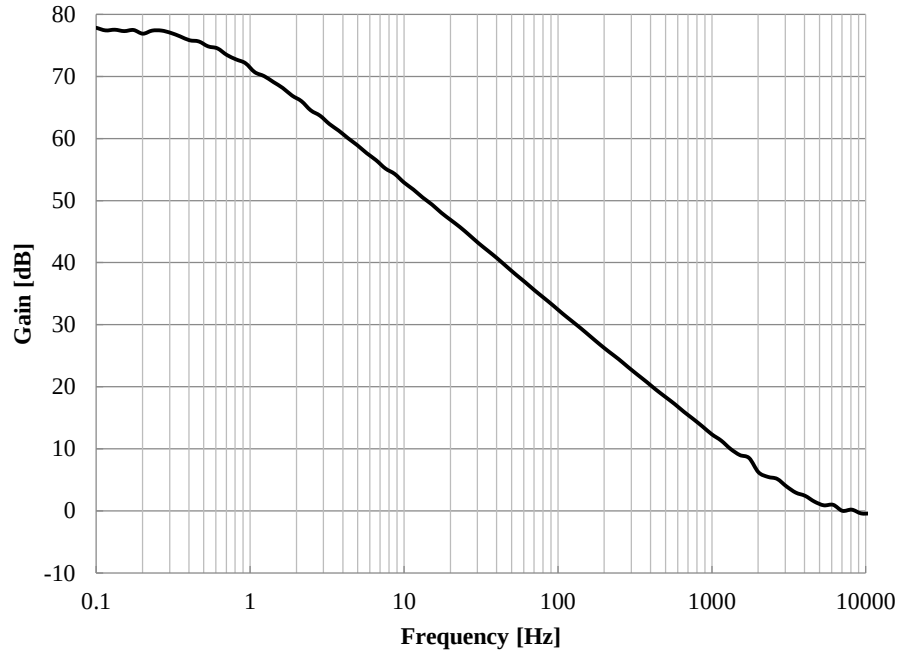
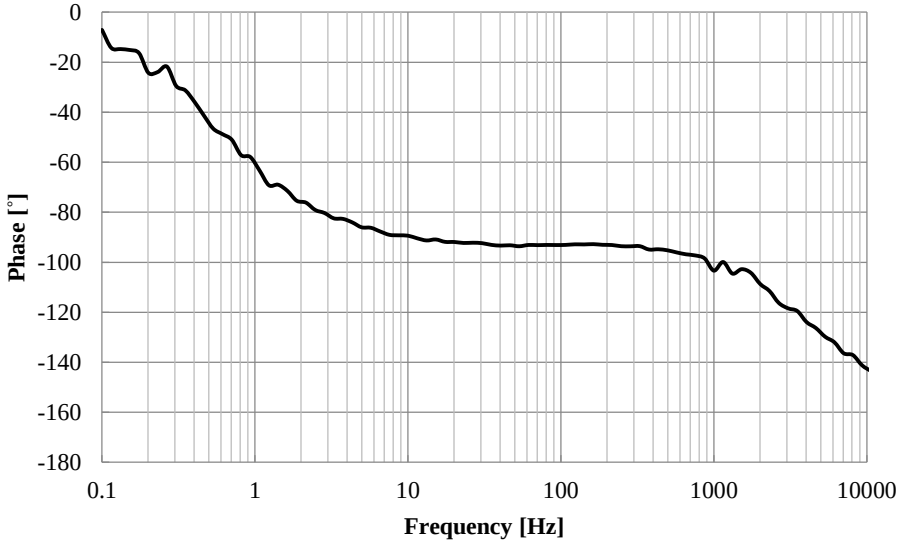


Fig. 3.17. Measured rail-to-rail input (yellow line) and output (blue line) waveforms with a 0.5-V supply voltage [18].

We used the ZGA5920 gain-phase analyzer to measure the open-loop frequency response. Fig. 3.18 shows our gain-phase analysis results. Our op-amp obtained a DC gain of 77 dB at the common-mode input voltage of 0.25 V. The unity-gain frequency was 4.0 kHz and the phase margin was 56° with a capacitive load of 40 pF. The current consumption was 140 nA, including all bias circuits.



(a)



(b)

Fig. 3.18. Measured open-loop frequency response. (a) Gain. (b) Phase [18].

Fig. 3.19 shows the DC gains and common-mode input voltages. For common-mode input voltages at 50 and 450 mV (i.e., at 50 mV from each supply rail), the DC gains of more than 40 dB were obtained.

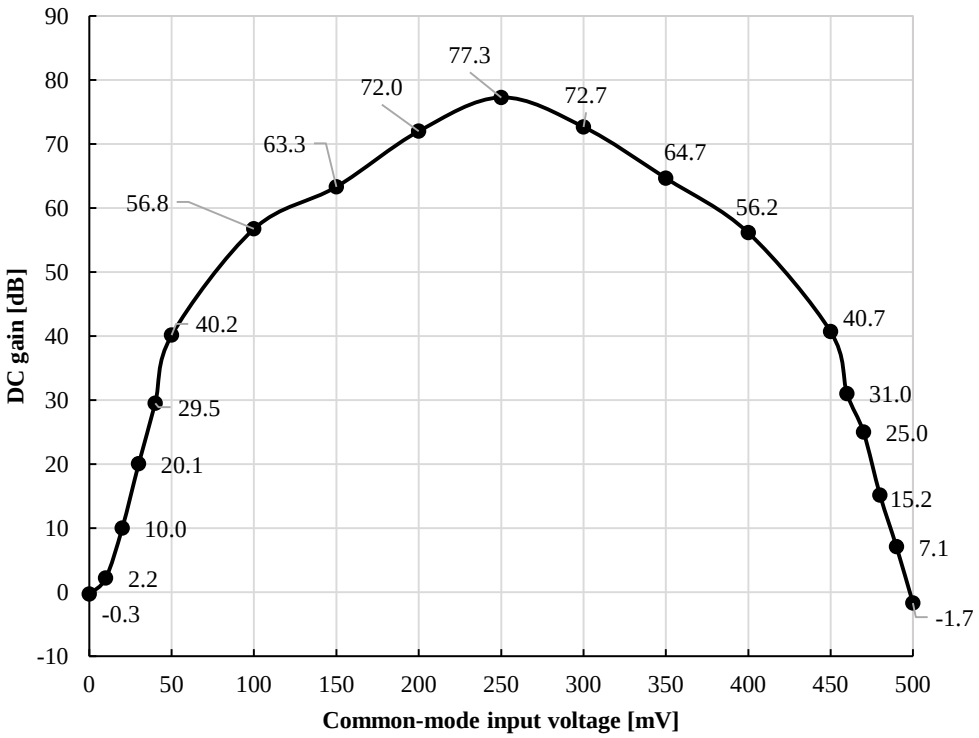


Fig. 3.19. Measured DC gain and common-mode input voltage [18].

We measured the common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) of the proposed circuit shown in Fig. 3.2. With a supply voltage of 0.5 V, CMRR was 55 dB for the common-mode input voltages of 0 and 0.5 V. PSRR was 52 dB for the supply voltages ranging 0.5−1.0 V.

Furthermore, the measured offset voltages were −0.8, −4.4, −6.2, and −7.8 mV (four samples). And the slew rate of the op-amp was 2 V/ms for both the rise and fall.

The figure of merit (FoM) of the op-amp was calculated using the conventional equation described as follows [4]:

$$FoM_1 = \frac{UGF \cdot C_L}{I_{total}}, \tag{3.6}$$

where UGF is the unity-gain frequency, CL is the load capacitance, and Itotal is the current consumed in the entire circuit. Thus, the FoM1 of our proposed circuit (including all bias and reference circuits) was 1143 with a load capacitance of 40 pF. Here, to include the effect of the phase margin for fair comparison, we also adopted another FoM equation described as follows [12]:

$$FoM_2 = \frac{UGF \cdot C_L}{I_{total}} \cdot \left(\frac{\tan \phi_M}{\tan 60^\circ} \right), \tag{3.7}$$

where ϕ_M is the phase margin of the op-amp. Then, the FoM2 of our circuit was 978.

TABLE II SUMMARY OF SIMULATION AND EXPERIMENTAL RESULTS [18]

	Simulation results	Experimental results
Supply voltage [V]	0.5	0.5
DC gain [dB]	101	77
Unity-gain frequency [kHz]	8.2	4.0
Load capacitance [pF]	40	40
Phase margin [˚]	50	56
Supply current [nA]	170	140
Power [nW]	85	70
FoM_1 [MHz pF/mA]	1929	1143
FoM_2 [MHz pF/mA]	1328	978

Table II summarizes the simulation and experimental results of the proposed op-amp. Table III summarizes the experimental results of the proposed circuit and those of the previously reported low-voltage op-amps. Our op-amp shows a large FoM, occupies a relatively small chip area, and has a rail-to-rail input/output feature operating with a supply voltage of 0.5 V. Moreover, high FoM values were obtained in [4] and [8]. However, these two op-amps do not have the rail-to-rail input/output feature. With a supply voltage of 0.5 V or less, the rail-to-rail operation is only available in [6], [9], and this work.

TABLE III SUMMARY OF EXPERIMENTAL RESULTS AS COMPARED TO PREVIOUSLY REPORTED LOW-VOLTAGE OP-AMPS [18]

	This work	[1]	[2]	[3]	[4]	[13]	[14]	[15]
Supply voltage [V]	**0.5**	1.0	0.5	0.9	0.5	1.0	1.0	0.25
Technology	**0.18 μm**	2 μm	0.18 μm	2.5 μm	0.18 μm	0.35 μm	0.35 μm	0.13 μm
DC gain [dB]	**77**	49	62	79	62	76	88	60
Unity-gain frequency [kHz]	**4.0**	1,300	10,000	5.6	102	8,100	11,670	1.9
Load capacitance [pF]	**40**	22	20	12	20	17	15	15
Phase margin [°]	**56**	57	N/A	62	52	N/A	66	53
Supply current [μA]	**0.14**	300	150	0.5	3.0	358	197	0.072
Power [μW]	**0.07**	300	75	0.45	1.5	358	197	0.018
Slew rate (rise) [V/μs]	**0.002**	0.7	2	N/A	0.035	2.74	2.53	0.0006
Slew rate (fall) [V/μs]	**0.002**	1.6	N/A	N/A	0.032	5.02	1.37	0.0008
CMRR [dB]	**55 @ DC**	N/A	75 @ 5 kHz	59 @ DC	N/A	71 @ DC	40 @ DC	N/A
PSRR [dB]	**52 @ DC**	61 @ 10 kHz	81 @ 5 kHz	N/A	N/A	45 @ DC	40 @ DC	N/A
Area [mm^2]	**0.036**	1.514	0.017	0.5	0.006	0.053	0.157	0.083
FoM_1 [MHz pF/mA]	**1,143**	95	1,334	134	680	385	889	392
FoM_2 [MHz pF/mA]	**978**	85	–	146	503	–	1,152	303
Rail-to-rail input/output	**YES**	YES	NO	YES	YES	YES	NO	YES

Chapter 4

Ultra-Low-Voltage and Ultra-Low Current Reference Circuit

In analog circuits, the current reference circuit influences on various features of the whole circuit. A resistor-less current reference circuit for ultra-low-voltage and ultra-low current circuits is proposed in this chapter.

This chapter describes a 0.6-V current reference circuit for use in ultra-low-power applications. In a conventional beta multiplier current reference circuit, a MOSFET that operates in the strong inversion and triode regions is used as a resistor. Our proposed circuit provides a forward body-biasing for the MOSFET to lower its threshold voltage and make it operate in its strong inversion region even at a very low supply voltage of 0.6 V. We ran simulations using SPICE parameters for a 0.18-μm standard CMOS process.

At a supply voltage of 0.6 V, the reference current was 2 nA. The chip area of the proposed current reference circuit was 0.022 mm^2.

4.1 Early Work and Applications

As the requirement about battery operations of handheld devices increases, the digital increases which about portable electronic devices, such as smart phones and tablets. And the demand for efficient low-power circuits increases rapidly. The current reference circuit is one of the most important parts in analog and mixed circuit systems. It generates reference current, which is used for op-amps, oscillators, phase-locked loops and, A/D and D/A converters, etc [10], [20-21].

CMOS analog integrated circuit, operated in the weak region, with has been draw much attention because of its potential in low operating voltage and low power consumption. The dedicated special circuit structure in order to the special requirements of analog integrated circuits.

Low-voltage, low-current reference circuits have been reported [19-35]. Circuits of ref [20-29] operate at a supply voltage over 1 V. Circuits of refs. [30-35] operate at a supply voltage of 1 V or less, however reference currents of refs. [31, 33] are over 50 nA. Circuits with reference currents of only several nano-amperes have also been reported [24, 29, 30].

A conventional current reference circuit (Beta-multiplier current reference circuit [20]) is show in Fig. 4.1. P-channel MOSFETS M1 and M2 forms a current mirror. When N-channel MOSFETS M3 and M4 operate in weak inversion region, the source voltage of M3 is given by:

$$\mathrm{V_{SM3}} = U_T \ln\left(\frac{S_{M3} S_{M2}}{S_{M4} S_{M1}}\right) \tag{4.1}$$

where U_T = kT/q is the thermal voltage, and S_{M1}–S_{M4} are aspect ratios of M1 – M4 [20]. V_{SM3} is equal to the voltage difference across the resistor R. The area of the resistor R becomes very large. The reference current I_{REF} is therefore given by the following equation:

$$I_{\mathrm{REF}} = \frac{U_T}{R} \ln\left(\frac{S_{M3} S_{M2}}{S_{M4} S_{M1}}\right) \tag{4.2}$$

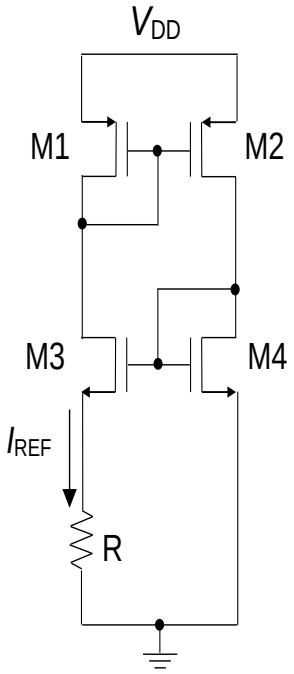


Fig. 4.1. Beta-multiplier current reference circuit [20].

A nano-ampere order of magnitude of the current reference circuit as show in fig. 4.1 needs hundreds of mega-ohm resistor elements, and it is hard to realize it in integrated circuits.

In order to solve this problem, Oguey and Aebischer proposed a circuit in which a resistor was replaced by a MOS transistor as shown in fig. 4.2 [10]. In

other word, a circuit was proposed in which the resistor R was replaced by an NMOS operating in strong inversion region and ohmic region. NMOS transistor M5 operates in its strong inversion and triode region. N-channel MOSFETs M3 and M4 operate in weak inversion. A chip area can be made smaller than a circuit using resistive elements.

However, the output voltage is 0.5 V of one unit solar cell, under such a low supply voltage, it is difficult to realize that the NMOS transistor M5 works in strong inversion region.

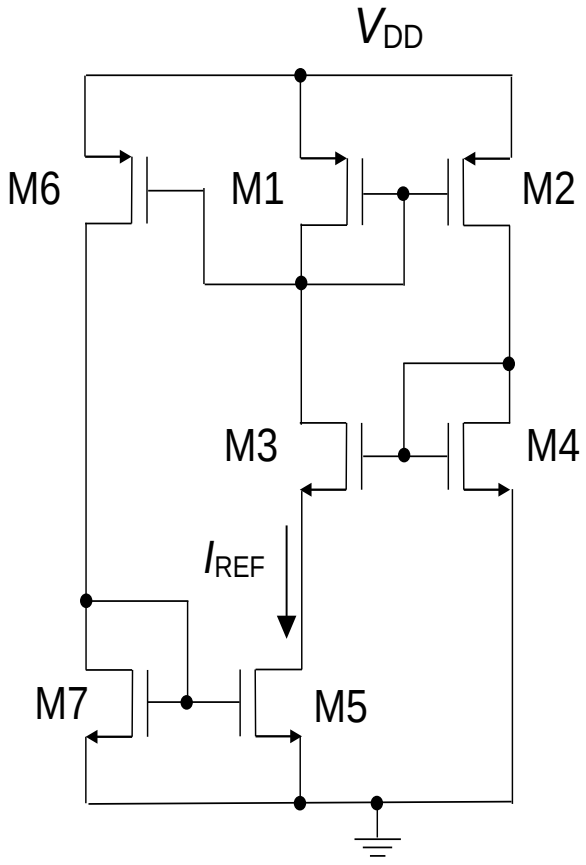


Fig. 4.2. Resistorless current reference circuit [10].

A 0.5-V operational amplifier was been proposed [18]. That paper used the Oguey bias circuit to generate a reference current of 2 nA. Without using a resistor, a supply-voltage-independent current-reference circuit is realized. The current reference circuit takes the place of the MOS transistor resistance element which works on the weak inversion region.

However, at a supply voltage of 0.5V or 0.6 V, NMOS transistor M5 operates in its weak inversion region, unless a special process with a low threshold voltage is used. The resistance linearity of this NMOS transistor then becomes worse than in the strong inversion region.

In the weak inversion region, the drain current of the NMOS transistor M5 is given by the following equation:

$$\mathrm{I_D} = I_0 \frac{W}{L} exp\{\frac{q(V_{GS}-V_T)}{nkT}\}\left\{1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right\}, \tag{4.3}$$

where I_o is the process-dependent parameter, and n is the slope factor. The drain conductance is given as follows:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} = \frac{q}{kT} I_0 \frac{W}{L} exp\{\frac{q(V_{GS}-V_T-nV_{DS})}{nkT}\}. \tag{4.4}$$

Therefore, the MOSFET drain resistance can be expressed as following:

$$R = \frac{\partial V_{DS}}{\partial I_D} = \frac{kT}{q}\frac{1}{I_0}\frac{L}{W} exp\{\frac{-q(V_{GS}-V_T-nV_{DS})}{nkT}\}. \tag{4.5}$$

From Eqs. (1) and (5), the reference current IREF can be given by the following equation:

$$I_{\mathrm{REF}} = I_0 \frac{W}{L} \ln\left(\frac{S_{M3}S_{M2}}{S_{M4}S_{M1}}\right) exp\left\{\frac{V_{GS}-V_T-nV_{DS}}{nU_{\mathrm{T}}}\right\} \tag{4.6}$$

In Eq (6), the exponential term contains a thermal voltage UT = kT/q, and therefore the reference current IREF depends on the temperature when the NMOS transistor M5 operates in the weak inversion region.

It is possible to reduce the temperature dependence of the current if the resistance of NMOS transistor M5 has the PTAT characteristics.

However, the circuit is dependent on the temperature exceedingly and there is such a big total area. The layout of the 2-nA current reference circuit is shown in Figure 4.3. Although the line regulation is 47.5%/V, this is a big problem to be solved. When the power supply voltage of the circuit in Fig. 4.2 is lowered to about 0.6 V, it becomes difficult to operate the NMOS in the strong inversion region acting as a resistance.

The layout of the beta-multiplier current reference shown in Fig. 4.2 is shown in Fig. 4.3. The area of the conventional circuit was 0.011 mm^2.

In order to solve the problem, we propose a circuit that provides a current of 2 nA with a supply voltage of 0.6 V.

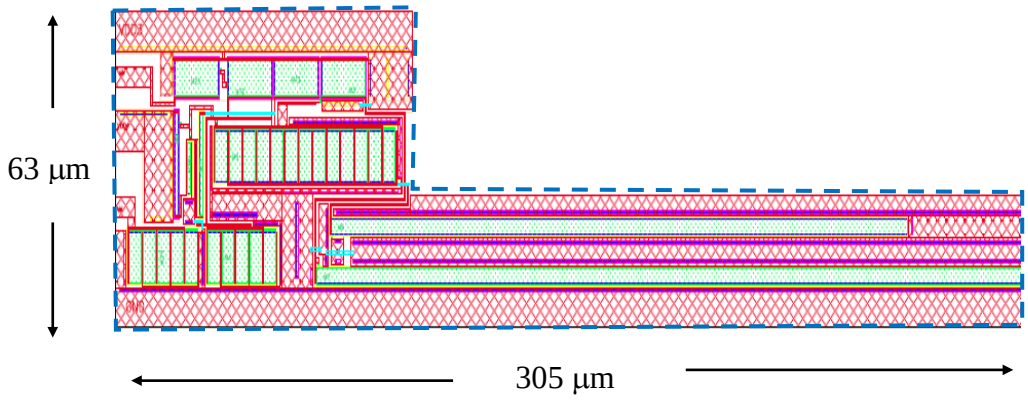


Fig. 4.3. Layout of the conventional current reference circuit (Fig. 4.2).

4.2 Proposed low-voltage current reference circuit

Fig. 4.4 shows the proposed current reference circuit. In the proposed circuit, the threshold voltage is lowered by using the body-bias effect so that M5 can

operate easily in the strong inversion region.

Furthermore, CMOS current reference circuit with simple structure has been configured using basic current mirror technique. PMOS transistors M1 and M2 constitute a current mirror. NMOS transistors N3 and M4 operate in weak inversion region. PMOS transistor M6 and NMOS transistor M7 provide a gate voltage for NMOS transistor M5. In order to realize an ultra-low-voltage operation, all transistors except NMOS transistor M5 operate in their weak inversion regions. Moreover, the linear region of NMOS transistor M5 becomes larger in strong inversion regions. In an alternative circuit, load device M5 has its body connected to its gate and is biased to operate in the strong inversion region. Since the source and the body of the MOS transistor M7 are both connected to the ground, there is no substrate bias effect. However, the body of the transistor M5 is connected to the gate. It becomes forward biased.

The body potential of the transistor M5 is higher than that of the body terminal connected to ground. Body-voltage value is greater than zero. As a result, the phenomenon caused the transistor M5 substrate bias effect, the threshold voltage of transistor M5 is lower than that of the transistor M7. In other words, threshold voltage gets lowered because the forward bias is applied to the body terminal of M5.

The body terminal of M5 is now connected to its gate terminal, which is enabled by a deep n-well, electrically separating the p-well of M5 from the p-type substrate. By applying a forward bias voltage between the body and source terminals of M5, the threshold voltage of M5 can be reduced. Hence, M5 can operate in the strong inversion region at ultra-low supply voltages such as 0.6 V.

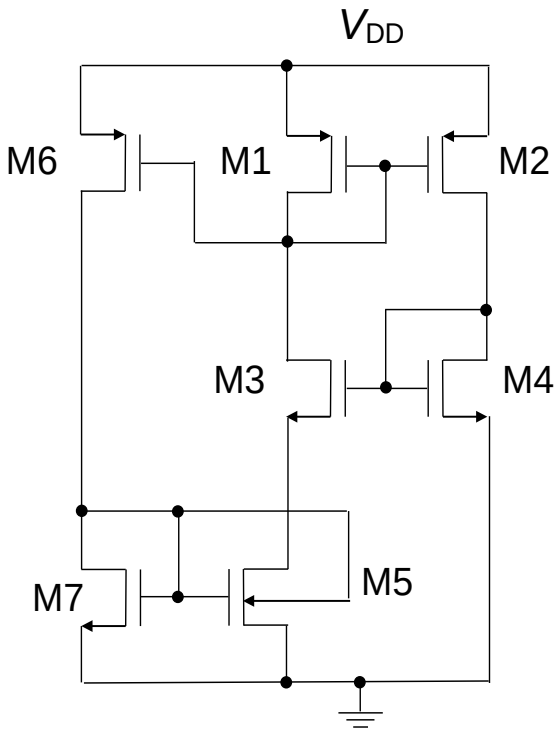


Fig. 4.4. Proposed CMOS current reference circuit

Since the reference current is in the order of nano-amperes, the gate lengths of MOSFETs M5 and M7 have to be several hundred micrometers.

Furthermore, in the proposed circuit, the threshold voltage of M5 can be reduced by body-biasing; hence, its gate length can be a few times larger than that in the conventional circuit shown in Fig. 4.2. Therefore, we adopted the self-cascode structure for M5 and M7 as shown in Fig. 4.5 to reduce the gate lengths and make the layout compact.

The layout of the proposed current reference circuit is shown in Fig. 4.6, and its area is 0.022 mm^2.

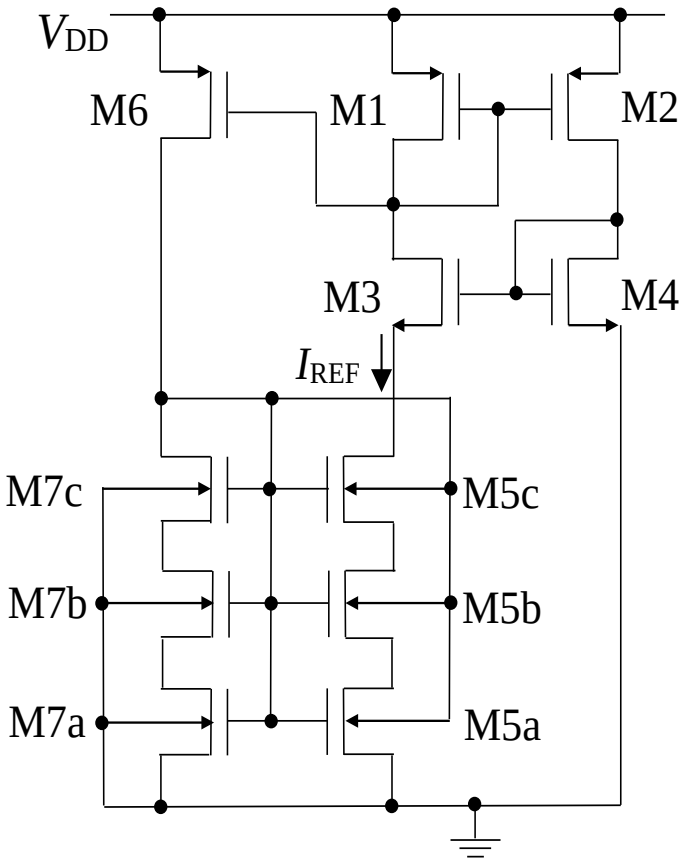


Fig. 4.5. Proposed current reference circuit using the self-cascode structure.

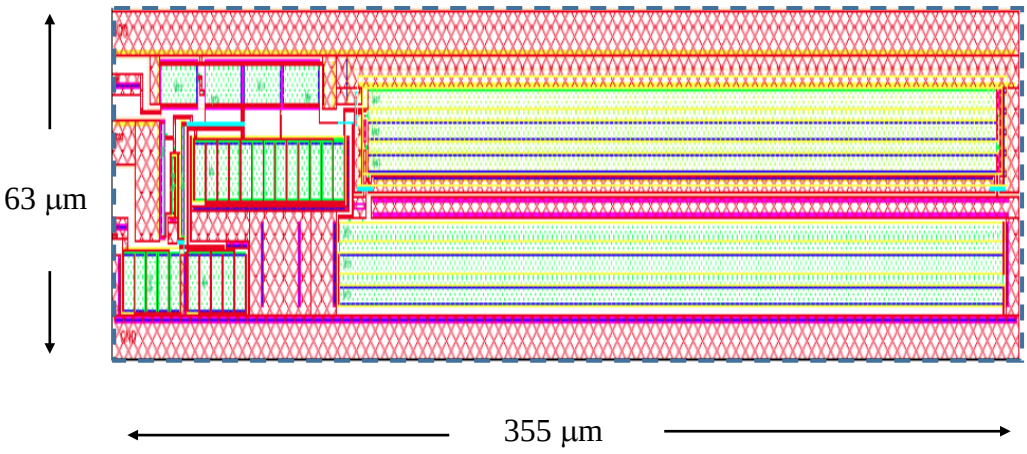


Fig. 4.6. Layout of the proposed current reference circuit.

4.3 Simulation Results and Layout

To verify the effectiveness of the proposed circuit, We ran HSPICE simulations for the proposed circuit shown in fig. 4.6 using BSIM3v3 SPICE parameters for a standard 0.18-μm CMOS process. Supply voltage is 0.6 V. The threshold voltages for PMOS and NMOS are approximately -0.4 V and 0.45 V, respectively. Fig. 4.7 shows reference current of the proposed circuit (Fig. 4.5) and conventional circuit (Fig. 4.2) for the supply voltage ranging from 0 to 1.8 V. The minimum supply voltage of the proposed circuit was 0.6 V and the reference current was 1.96 nA. The total power consumption is 3.5 nW at a supply voltage of 0.6 V. On the other hand, the minimum supply voltage of a conventional circuit shown in Fig. 4.2 was 0.8 V.

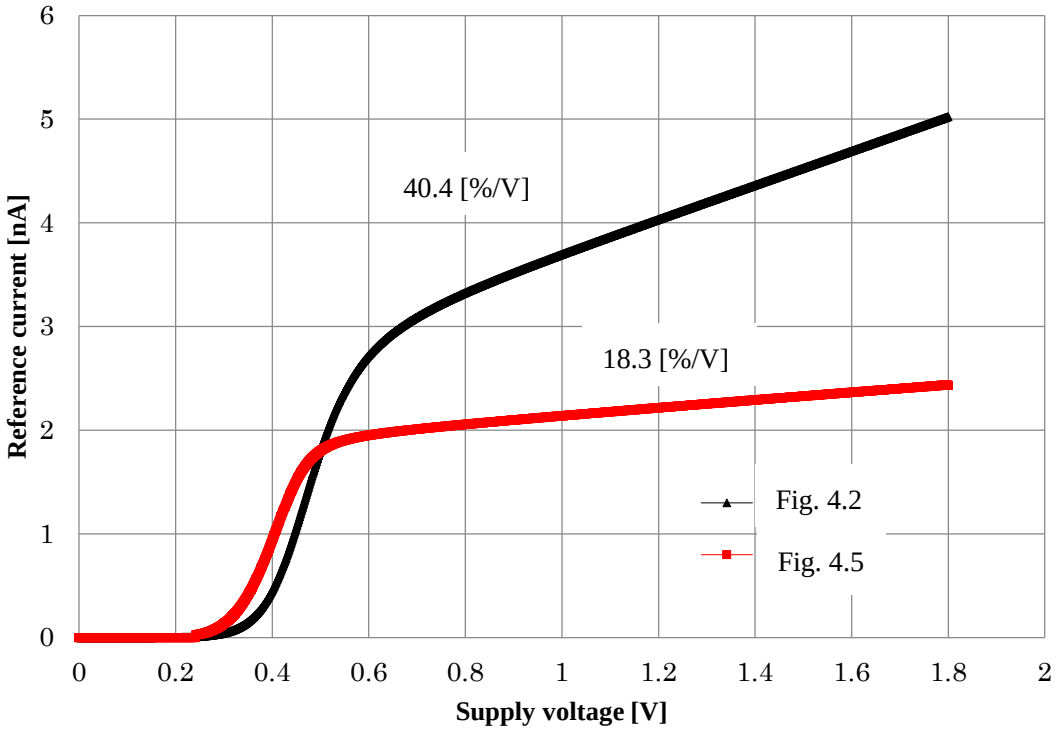


Fig. 4.7. The line regulation of conventional current reference circuit.

As show in fig. 4.7, the line regulation of conventional current reference circuit Fig. 4.2 is 40.4 %/V, while the proposed current reference circuit Fig. 4.5 is reduced to 18.3 %/V with the supply voltage changed from 0.6 V to 1.8 V. Notice that a parasitic p-n diode current between the body and source of M5 is about 10% at a supply voltage of 0.6 V. Table IV summarizes the simulation results of the conventional circuit at supply voltage of 0.8 V and proposed circuit at supply voltage of 0.5 V and 0.6 V.

TABLE IV SUMMARY OF SIMULATION RESULTS

	Conventional circuit (Fig. 4.2)	Proposed circuit (Fig. 4.5)	
Supply voltage [V]	0.8	0.5	0.6
Reference current I_{REF} [nA]	3.3	1.84	1.96
Total power consumption [nW]	8.0	2.6	3.5
Line regulation [%/V]	40.4	22.3	18.3
Chip area [mm^2]	0.011	0.022	0.022

Table V summarizes the simulation results of the proposed circuit and those of the previously reported low-voltage current reference circuits. The minimum supply voltage of our proposed circuit was 0.6 V, which was 0.2 V lower than those of previously reported circuits. Note that the minimum supply voltage of our proposed circuit was 0.25 V lower than the sum of the threshold voltages, VTN + | VTP |.

The line regulation of the proposed current reference circuit was 18.3 %/V for a supply voltage ranging from 0.6 V to 1.2 V. It should be noted that the parasitic

p–n diode current between the body and source of M5 was approximately 10% of the drain current of M5 (I_{REF}) at a supply voltage of 0.6 V.

One of the issues noted was that the temperature coefficient (TC) of the proposed circuit was much higher than those of the other circuits. The reason is surmised that NMOS transistor M5 in Fig. 4.2 (and M5a-c in Fig. 4.5) is in the moderate inversion region rather than completely in the strong inversion region, and the reference current is largely affected by temperature. This is the issue that we intend to improve in future.

TABLE V SUMMARY OF THE SIMULATION/EXPERIMENTAL RESULTS AS COMPARED TO PREVIOUSLY REPORTED REPORTED CIRCUITS [19]

	Proposed circuit **	[22]*	[24]*	[30]**	[31]*	[34] **
Minimum supply voltage [V]	**0.6**	1.25	1.3	0.85	0.8	0.8
Technology [μm]	**0.18**	0.18	0.35	0.18	0.18	0.18
V_{TN} + | V_{TP} | [V]	**0.85**	-	-	0.87	-	-
Reference current I_{REF} [nA]	**2.0**	92.3	9.95	2.05	54.1	20
Total power consumption [nW]	**3.5 @0.6V**	670 @1.8V	88.5 @1.3V	5.1 @0.85	289 @1V	120 @0.8V
Temperature (°C)	**−40 to 80**	−40 to 85	−20 to 80	-	0 to 80	−40 to 65
TC (ppm/°C)	**26,015**	177	1,190	91	63	-
Line regulation [%/V]	**18.3**	7.5	0.046	1.35	0.21	-
Chip area [mm^2]	**0.022**	0.001	0.12	-	0.245	-
Year	**2017**	2016	2010	2010	2013	2016

*experimental results, **simulation results.

Chapter 5

Conclusions

We developed and fabricated a 0.5-V rail-to-rail operational amplifier (op-amp) with ultra-low-power operation in a 0.18-μm standard CMOS process. The op-amp has a two-stage structure that comprises a complementary input stage and a novel cross-coupled output stage. The cross-coupled output stage increases the transconductances of the MOSFETs of the output stage without requiring additional chip area. Hence, it increases the gain of the op-amp and drivability for a capacitive load. Our experimental results showed that the DC gain was 77 dB at the common-mode input voltage of 0.25 V with a supply voltage of 0.5 V. DC gains of more than 40 dB were obtained for common-mode input voltages ranging 50−450 mV. Furthermore, the unity-gain frequency was 4.0 kHz and phase margin was 56° with a capacitive load of 40 pF. The power consumption was 70 nW including all bias circuits.

In addition, a resistor-less reference circuit for ultra-low-voltage and ultra-low current large-scale integrations is proposed. It operates in nano-ampere orders of current under the condition such that the power supply is less than 1 V. Under a voltage of 0.6 V, it can provide a current of 2 nA. In order to reduce the NMOS transistor’s gate-source voltage and the threshold voltage, we connect the gate terminal with body terminal. And we use the deep well process in the standard process. The line regulation of proposed low-voltage current reference circuit is reduced to 18.8%/V with the supply voltage changed from 0.6 to 1.8 V. To

reduce the threshold voltage of the NMOS transistor acting as a resistor and make it operate in the strong inversion region, we connect its body terminal with the gate terminal. HSPICE simulation results show that the minimum supply voltage is 0.6 V, which is 0.2 V lower than those of previously reported circuits. The total power consumption is 3.5 nW at a supply voltage of 0.6 V. The layout design uses the Cadence layout software, uses optimized the layout design technique to carry on the design, the area of layout is 0.022 mm^2.

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